ORIGINAL ARTICLE

Fabrication Suspended High-Aspect-Ratio Parylene Structures for Large Displacement Requirements

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Abstract: A new method is presented for the fabrication of suspended parylene structures, using dry etching at low temperatures with a single standard silicon wafer. A silicon micro trench is used as a mold, in which parylene beams are fabricated through the deposition and removal of parylene in multiple stages, after which the structure is released from the same side of the silicon wafer. Compared to traditional processes, this approach eliminates the deposition of unnecessary silicon-dioxide, overcomes the need for double-sided micro-machining and supports the wafer during the release of the structure, thereby reducing process complexity and production costs. The proposed process is used to fabricate a test device of free-standing parylene beams 20 *um* in width, 3000 *um* in span, and 50 *um* in thickness to verify the feasibility of the structure based on suspended parylene. The ductile characteristics of the parylene beams allows elastic deformation of up to 100 *um*. CoventorWare simulation results show that parylene generates only 2.3% of the maximum Von Mises stress compared to a silicon based test device with the same dimensions. This new process is well-suited for applications to devices with large in-plane displacement and low stiffness.

Keywords: Parylene; suspended structures; MEMS

I. Introduction

Suspended structures are widely used as transducers in Micro-Electro-Mechanical Systems (MEMS). Soft beams with limited stiffness in the in-plane direction are required to provide a high degree of sensitivity. Traditional MEMS devices such as accelerometers [1, 2] and optical switches [3, 4] are produced with single crystal silicon (SCS); however, the large Young's modulus (~150GPa) of this material prevents the creation of soft beams. One alternative approach to producing softer beams is the use of softer materials.

Polymer MEMSs have attracted a great deal of attention in recent years for sensing, actuating, and providing structure in a wide range of applications, including physical transduction, chemical analysis, and medical care [5]. The ease of fabrication at low temperatures combined with unique mechanical flexibility makes polymeric devices a promising alternative to silicon-based devices.

Among the variety of polymer materials available, parylene (poly-para-xylylene) has been most broadly used thanks to its high flexibility (Young's Modulus ~4.7GPa [6]), ductility with large linear-elastic range (yield strain ~3 %), 30% lower TCE than SU-8 [7] or polyimide, chemical inertness, and bio-compatibility. Parylene is compatible with microfabrication technologies is suitable for deposition using pinhole-free conformal chemical vapor deposition (CVD) coating at room-temperature, and can be dry-etched using oxygen plasma [6]. These features provide parylene processes with a high degree of compatibility in conventional microfabrication techniques. Parylene MEMS technology has been under development for nearly ten years. Of the three most common parylenes (Figure 1), parylene C is most commonly used in industry.

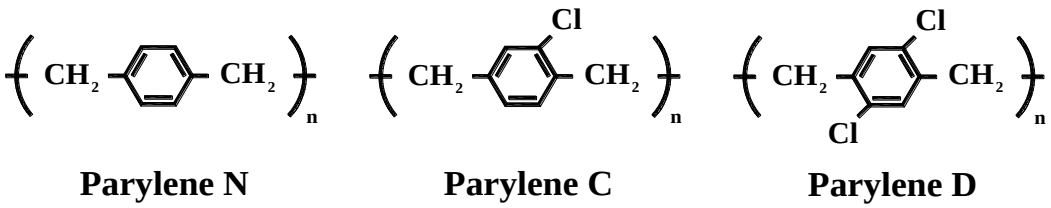

Figure 1. Schematic of chemical structures for the three most commonly employed parylenes.

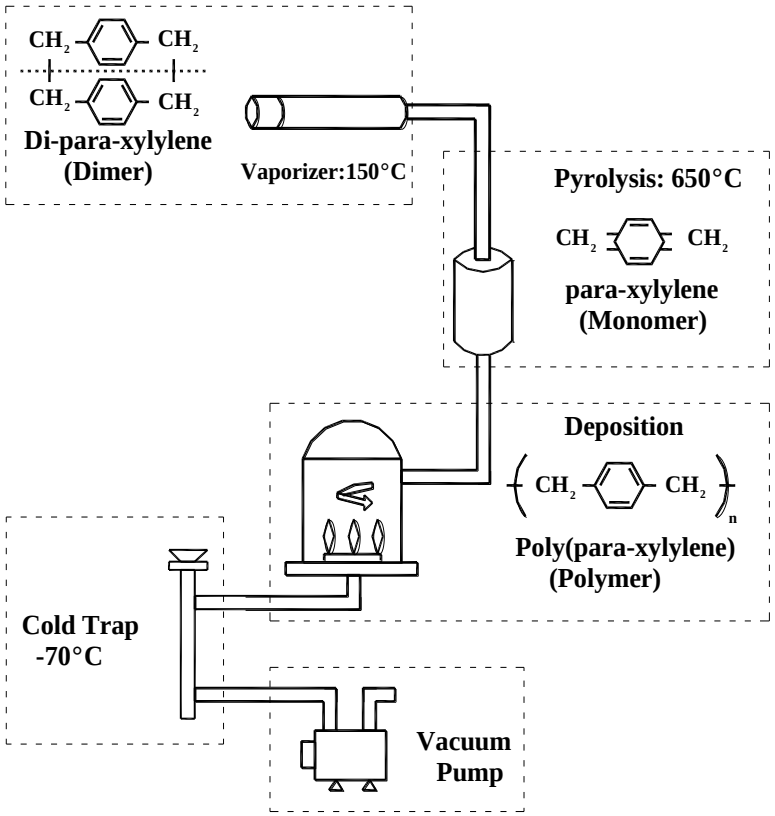

Figure 2. Schematic of parylene deposition process.

The process of parylene deposition [8] is illustrated in Figure 2. The parylene coater used in this work is adapted from the Deree Technologies Company. Parylene is deposited at room temperature at pressures of approximately 0.1 torr, with the mean free path of the molecules on the order of 0.1 *cm*. The first step in the deposition process is the vaporization of the solid dimmer by heating to 150 ^{o}C. The second step is the pyrolysis of the dimmer, cleaving at the two methylene-methylene bonds to yield stable monomeric radicals, para-xylyene at approximately 650 ^{o}C. The monomers are driven by a pumping system into the deposition chamber at room temperature, where they polymerize on the substrate. Finally, a cold trap at approximately -70 ^{o}C is used to collect the un-reacted monomers before they enter the pumping system.

Traditionally, parylene has been deposited as a coating in thin film materials. Suzuki et al. proposed the use of a silicon micro trench as a mold, in which parylene beams are produced through multi-stage deposition-removal [9], thereby extending the application of parylene by providing it with a high-aspect-ratio structure. Figure 3 shows the process of fabricating the parylene beams. Figure 3 (a) shows the etching of the silicon trench to create a micro mold for

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the deposition of parylene. In Figure 3 (b), due to step coverage effect during the deposition of parylene, the thickness in the corners of the trench is greater than that along the sidewall, increasing the likelihood of sealing the trench in a single run through the deposition of thick parylene layers. To prevent the sealing of the trench, oxygen plasma is applied to remove the uppermost parylene, thereby re-opening the trench, as shown in Figure 3 (c). After re-opening the trench, the second parylene layer is applied to fill the trench without voids, as shown in Figure 3 (d). The number of times that parylene must be deposited and removed is determined by the width of the trench. The creation of a larger parylene beam requires an increased number of repetitions to deposit and trim the parylene. Figure 3 (e) shows the process of removing the topmost section of parylene for the second time.

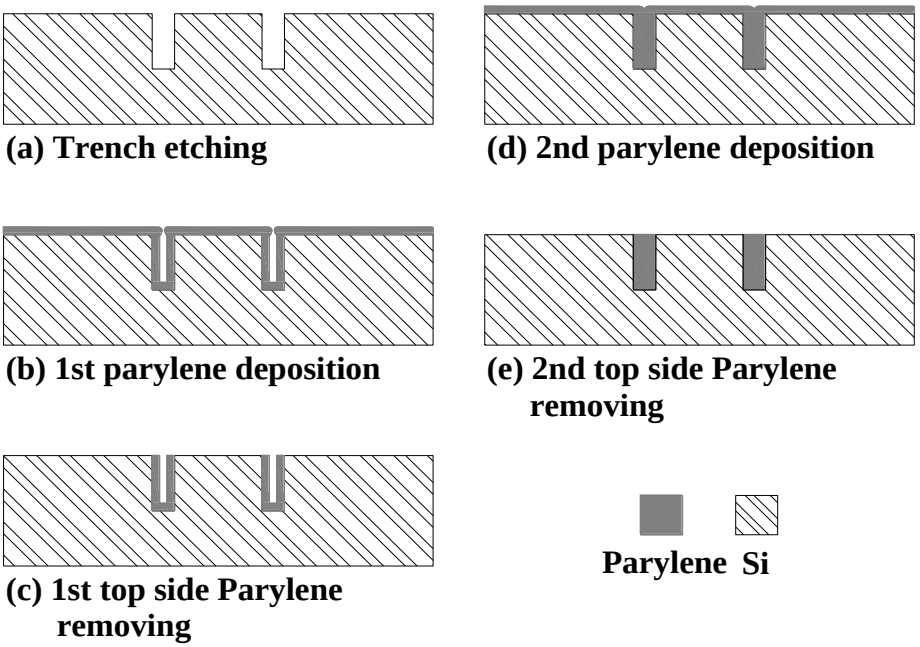


Figure 3. Schematic of method for fabricating parylene beams.

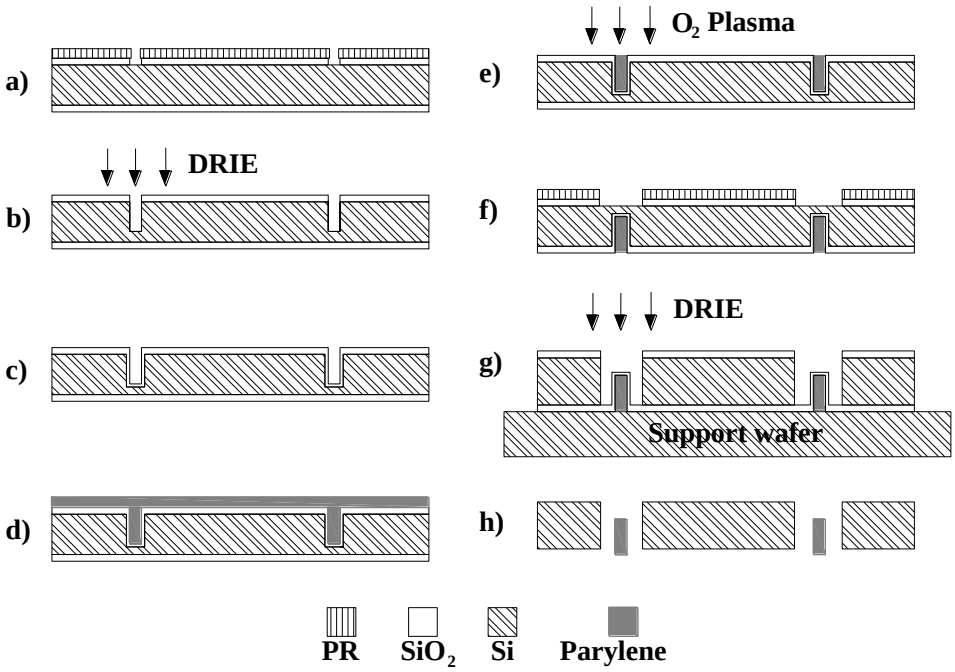


Figure 4. Traditional process flow for suspended parylene structures.

The traditional method for releasing the parylene structures [9] is illustrated in Figure 4, in which a double-sided silicon wafer is used as a substrate. This process uses patterned oxide as a mask for etching the trench. Following the creation of the trenches, a second course of oxidation is applied to the substrate to form an etch-stop layer (SiO_2) for the etching of later trenches. This is followed by multiple steps to deposit and remove the parylene, thus creating beams in the trenches. The substrate is then placed upside down to pattern the backside oxide as a mask. To allow for the etching and releasing of the wafer through the trench, the substrate is glued to the support wafer, and the substrate is etched away from the backside to expose the parylene beams, which are covered by etch-stop (SiO_2). Finally, the parylene beams are released by stripping off the SiO_2 with a buffered HF solution. This process requires high temperature oxidation, double-sided micro-machining, and a support wafer.

The parylene beams can also be released [6] using SOI wafer, where the parylene beams are released by stripping off the buried SiO_2 layer with a buffered HF solution. While the fabrication method is simple and straightforward, the cost of the wafer is much greater than that of single-crystal-silicon (SCS) wafer.

This paper proposes a simpler method for creating suspended parylene structures. Our process employs a single-sided polished silicon wafer as a substrate, and photoresist as an etching mask, and releases the parylene beams from the front side. This eliminates the creation of excessive thermal dioxide, overcomes the need for double-sided micro-machining and supports the wafer during the release of the structures, thereby reducing process complexity and production costs. Without the need for high temperature oxidation, the process can be performed within a low temperature environment, thereby eliminating the need to remove thermal oxide using buffered HF solution.

The remainder of this paper is organized as follows: the proposed process for fabricating suspended parylene structures is described in Section 2. Section 3 introduces a test device to create suspended parylene structures. Test results and measurements are presented in Section 4, and conclusions are presented in Section 5.

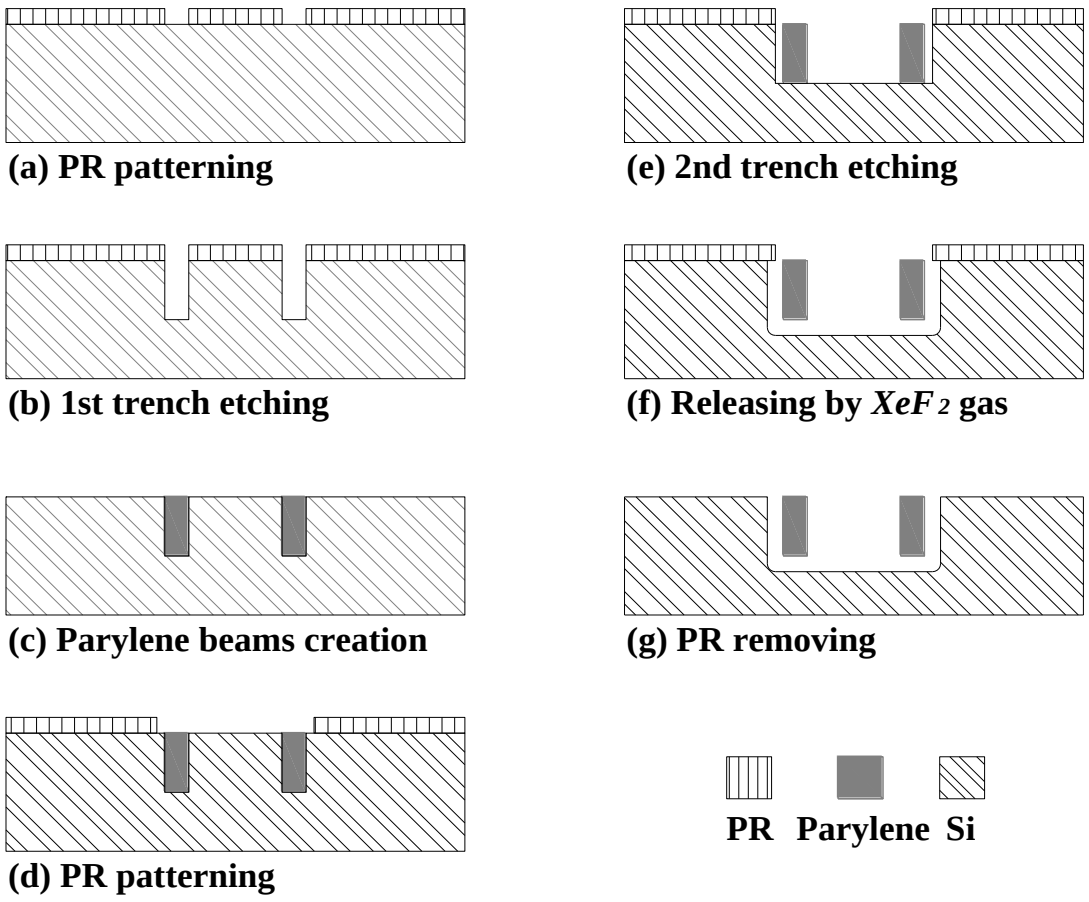


Figure 5. Proposed process flow for parylene structures: Step (a), photoresist patterning; Step (b), 1st trench etching; Step (c), fabrication of parylene beams; Step (d), photoresist patterning; Step (e), 2nd trench etching; Step (f), releasing structure; Step (g), photoresit removal.

II. Process flow for suspended parylene structures

The proposed process uses one single-sided polished silicon wafer as a substrate, with photoresist as an etching mask, thus thermal oxide is not required. The process is illustrated in Figure 5. In the first step, photoresist is spun on a silicon wafer as an etching mask for deep silicon etching, followed by a pattern transfer process. In step (b), inductively coupled plasma (ICP) etching is used to etch the silicon to a desired depth [10, 11]. The parylene is deposited in the trenches and trimmed repeatedly to create beams in the deep trenches in step (c). In step (d), photoresist is spun on the silicon wafer as an etching mask, followed by a pattern transfer process. The exposed silicon is etched to release the structure. In step (e), the exposed silicon is etched to a specific depth to facilitate the release of the structure. In step (f), XeF_2 gas is used to release the parylene based structures. In step (g), oxygen plasma is used to strip the photoresist.

III. Test structure design

To verify the feasibility of the suspended parylene-based structure, a sample is produced, as illustrated in Figure 6 (a). Due to the poor adhesion force between the parylene and silicon [12], parylene anchors are designed to plug into the silicon to enforce adhesion, as shown in Figure 6 (b). In this manner, the parylene beams could be moved easily by applying force to the middle part of the beams. The dimensions of the parylene beams are 3000 *um* in span, 20 *um* in width, and 50 *um* in depth following fabrication.

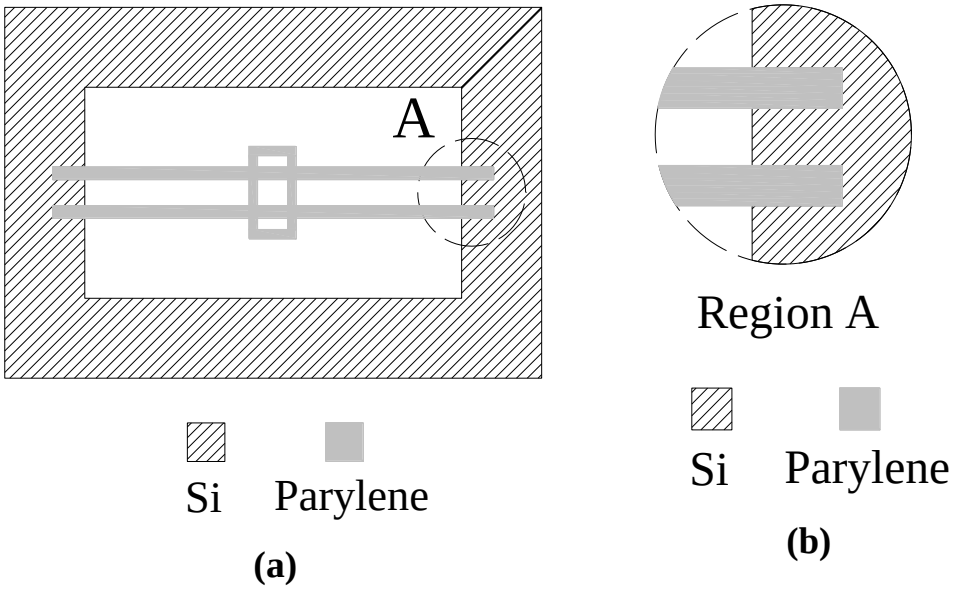


Figure 6. (a) Layout of test device for suspended parylene structure, (b) close-up view of anchor design.

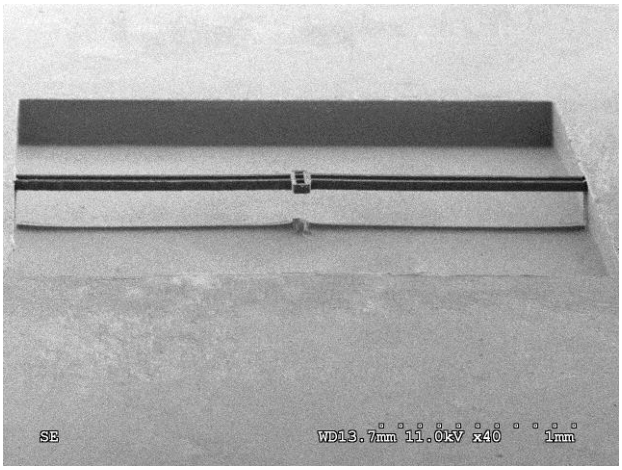
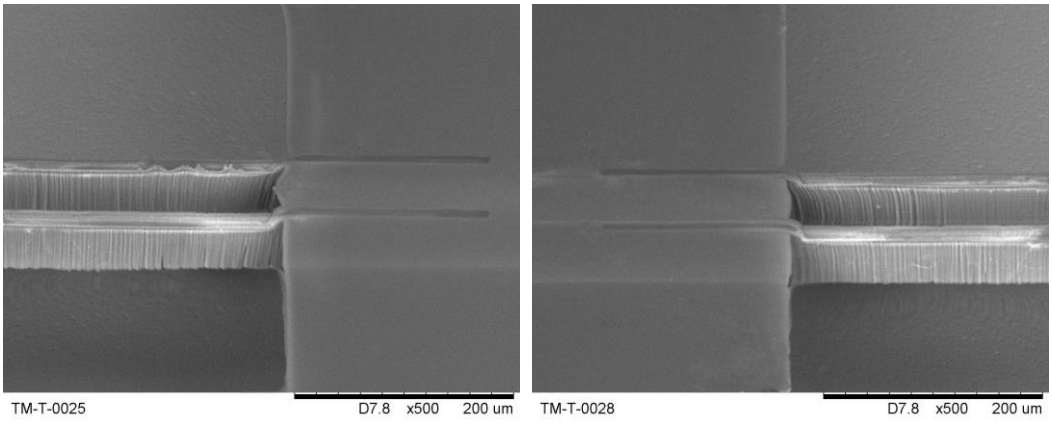
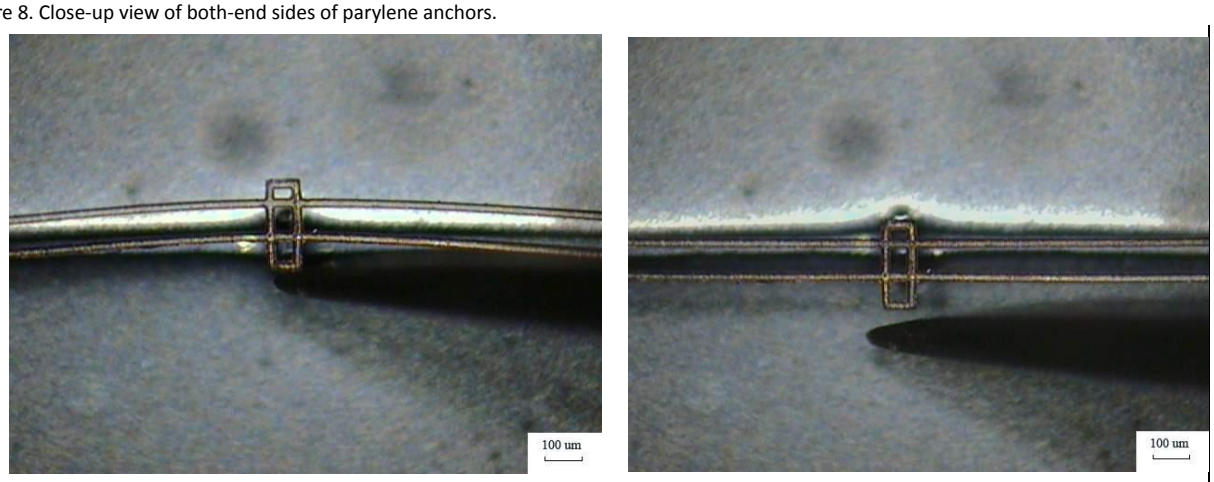


Figure 7. SEM photo of test device.



(a) (b)

Figure 8. Close-up view of both-end sides of parylene anchors.



(a) (b)

Figure 9. CCD photos of test device driven by probe tip (a) approximately 100 um of in-plane displacement, (b) releasing approximately 100 um of in-plane displacement.

IV. Results and Measurements

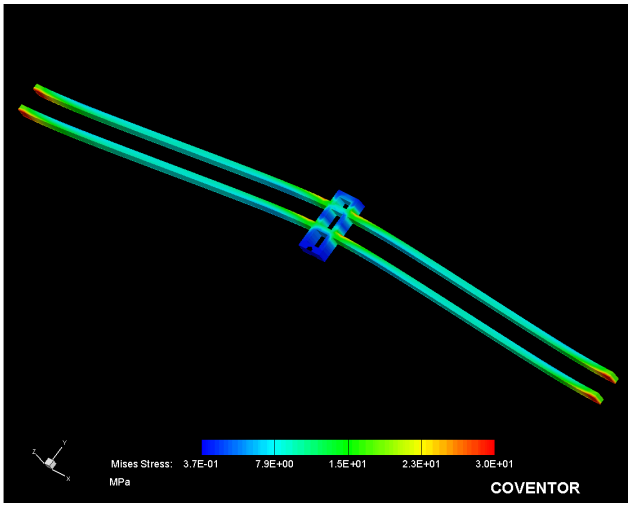
Figure 7 presents an SEM image of free-standing parylene structures, while Figures 8 (a) and 8 (b) respectively illustrate the right and left side close-up views of the parylene anchors. Figures 9 (a) and 9 (b) respectivley show CCD photos of the test device driving the tip of a probe causing 100 *um* of in-plane compression/release displacement. The Young's modulus of high-aspect-ratio of the parylene beam is about 4.7GPa [6], and that of single crystal silicon is about 150GPa. Compared to single crystal silicon, the parylene-based test device presents a high degree of elastic deformation. To evaluate the characteristics of ductility in the proposed devices, we simulate the maximum stress and stress distribution, and compare these values with those of silicon, the material traditionally used for MEMS. Using the same 100 *um* of in-plane displacement at the center of the device, Figures 10 (a) and 10 (b) respectively show the CoventorWare simulation results of stress distribution for parylene and silicon. The maximum Von Mises stresses are generated at the anchors for both materials. The parameters used in the simulations are illustrated in Table 1. Table 2 shows that the maximum Von Mises stresses of the simulation results are lower than their yield strength. The maximum Von Mises stress of the parylene-based test devices (30MPa) is only 2.3 % of that in silicon (1.3GPa). Parylene is a high-aspect-ratio structural material, well suited to use in devices with large in-plane displacements and low stiffness.

Table 1. Material properties of parylene C and Single Crystal Silicon (100) in test device simulations

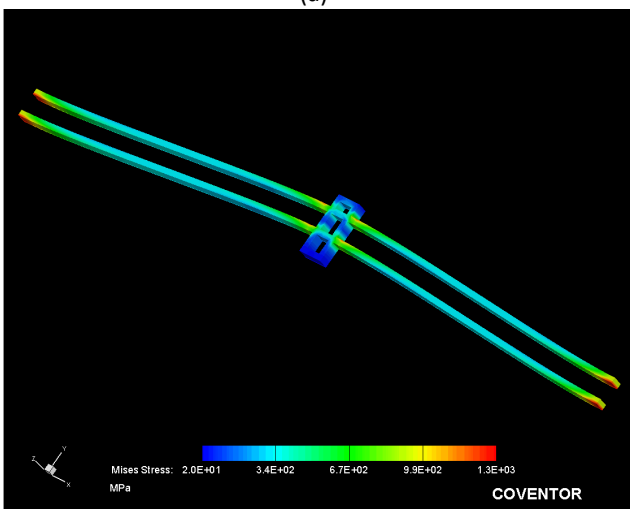
Material	parylene C	Single Crystal Silicon (100)
Yield Strength (*MPa*)	55 [13]	7000
Young's Modulus (*GPa*)	4.7 [6]	150
Poison ratio	0.4 [14]	0.17
Density (kg/m^3)	1289 [13]	2330

Table 2. Maximum Von Mises stresses of simulation results generated by the same 100 *m* of in-plane displacement at the center of for Single Crystal Silicon (100) and parylene test structures, respectively.

Material	Parylene C	Single Crystal Silicon (100)
Maximum Von Mises stress (*MPa*)	30	1300
Yield strength (*MPa*)	55	7000
Stress ratio (parylene/SCS)	2.3%	



(a)



(b)

Figure 10. Von Mises stress distribution of Coventorware simulation generated by 100 m of in-plane displacement at center of device for (a) parylene and (b) silicon.

V. Conclusion

A new process for fabricating suspended parylene-based structures is presented. The process uses a silicon micro trench as a mold, in which parylene beams are fabricated through the deposition and removal of parylene in multiple stages, after which the structure is released from the same side of the silicon wafer. Compared to traditional processes, this approach eliminates the deposition of unnecessary silicon-dioxide, overcomes the need for double-sided micro-machining and supports the wafer during the release of the structure, thereby reducing process complexity and production costs. Without the need for thermal oxide, the process can be performed at low temperatures without wet-etching. A test device is fabricated to verify the feasibility of the suspended parylene-based structure. The dimension of the free-standing test structures are 20 *um* in width, 3000 *um* in span, and 50 *um* in thickness. Thanks to the ductility characteristic of the parylene beams, the devices provide elastic deformation of up to 100 *um*. Coventorware simulation results show that the parylene generated only 2.3% of the maximum Von Mises stress compared to the same dimensions of a silicon-based test device. This new process is well suited for use in devices with large in-plane displacement and low stiffness.

VI. Acknowledgement

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